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Education Information

Doctorate, Syracuse University, Mühendislik Fakültesi, Bilgisayar Mühendisliği Bölümü, United States Of America 2001 - 2005

Postgraduate, Syracuse University, Mühendislik Fakültesi, Bilgisayar Mühendisliği Bölümü, United States Of America 1999 - 2001

Undergraduate, Selcuk University, Faculty Of Engineering, Elektrik Elektronik Mühendisliği Bölümü, Turkey 1993 - 1997

Foreign Languages

English, C1 Advanced

Dissertations

Doctorate, Reliability-centric system design for embedded systems, Syracuse University, Computer Engineering, 2005

Research Areas

Computer Sciences, Equipment, Logic Design, Engineering and Technology

Academic Titles / Tasks

Professor, Hacettepe University, Mühendislik Fakültesi, Bilgisayar Mühendisliği Bölümü, 2019 - Continues

Advising Theses

TOSUN S., Arıza kaldırabilir yonga-üstü-ağlar için topoloji oluşturma, uygulama eşleme ve yönlendirme algoritmalarının tasarlanması, Postgraduate, V.BABAEI(Student), 2015

TOSUN S., Hareketli kameralarda hareketli nesnelerin tespiti ve sınıflandırılması, Postgraduate, Ö.MERCANOĞLU(Student), 2015

TOSUN S., Örgü topoloji temelli yonga-üstü-ağlarda enerji tüketimini azaltacak uygulama eşleme tekniklerinin oluşturulması, Postgraduate, M.ÖZEN(Student), 2011

TOSUN S., Evrensel aydınlatmada kullanılan foton haritalama yönteminin paralelleştirilmesi, Postgraduate,

Published journal articles indexed by SCI, SSCI, and AHCI

- I. **Integer linear programming-based optimization methodology for reliability and energy-aware high-level synthesis**
DİLEK S., TOSUN S.
Microelectronics Reliability, vol.139, 2022 (SCI-Expanded)
- II. **Computation Power and Energy Optimized Task Allocation in Internet of Things**
Kazanci I., ÖZDEMİR S., TOSUN S.
IEEE Transactions on Network and Service Management, vol.19, no.4, pp.4424-4433, 2022 (SCI-Expanded)
- III. **A survey on computation offloading and service placement in fog computing-based IoT**
Gasmi K., DİLEK S., TOSUN S., Ozdemir S.
JOURNAL OF SUPERCOMPUTING, vol.78, no.2, pp.1983-2014, 2022 (SCI-Expanded)
- IV. **A High-Level Synthesis Methodology for Energy and Reliability-Oriented Designs**
Dilek S., Smri R., Tosun S., Dal D.
IEEE Transactions On Computers, vol.71, no.1, pp.161-174, 2022 (SCI-Expanded)
- V. **HAFTA: Highly adaptive fault-tolerant routing algorithm for two-dimensional network-on-chips**
Ipek A., TOSUN S., Ozdemir S.
CONCURRENCY AND COMPUTATION-PRACTICE & EXPERIENCE, vol.33, no.21, 2021 (SCI-Expanded)
- VI. **ILP formulation and heuristic method for energy-aware application mapping on 3D-NoCs**
Nalci Y., Kullu P., TOSUN S., ÖZTÜRK Ö.
JOURNAL OF SUPERCOMPUTING, vol.77, no.3, pp.2667-2680, 2021 (SCI-Expanded)
- VII. **Library Characterization of Arithmetic Circuits for Reliability-Aware Designs in SRAM-Based FPGAs**
Gokalan A., TOSUN S., DAL D.
JOURNAL OF ELECTRONIC TESTING-THEORY AND APPLICATIONS, vol.36, no.6, pp.743-756, 2020 (SCI-Expanded)
- VIII. **Mapping application-specific topology to mesh topology with reconfigurable switches**
Kullu P., AR Y., TOSUN S., ÖZDEMİR S.
IET COMPUTERS AND DIGITAL TECHNIQUES, vol.14, no.1, pp.9-16, 2020 (SCI-Expanded)
- IX. **Genetic Algorithm-based Reliability Optimization for High-Level Synthesis**
TOSUN S., Yaran T. T. G.
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, vol.28, no.3, 2019 (SCI-Expanded)
- X. **Energy-aware and fault-tolerant custom topology design method for network-on-chips**
Kullu P., TOSUN S.
NANO COMMUNICATION NETWORKS, vol.19, pp.54-66, 2019 (SCI-Expanded)
- XI. **Evolutionary task allocation in Internet of Things-based application domains**
Khalil E. A., Ozdemir S., TOSUN S.
FUTURE GENERATION COMPUTER SYSTEMS-THE INTERNATIONAL JOURNAL OF ESCIENCE, vol.86, pp.121-133, 2018 (SCI-Expanded)
- XII. **Energy-aware partitioning of fault-tolerant irregular topologies for 3D network-on-chips**
TOSUN S., Ajabshir V. B.
JOURNAL OF SUPERCOMPUTING, vol.74, no.9, pp.4842-4863, 2018 (SCI-Expanded)
- XIII. **Fault-Tolerant Topology Generation Method for Application-Specific Network-on-Chips**
TOSUN S., Ajabshir V. B., Mercanoglu O., OZTURK O.
IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol.34, no.9, pp.1495-1508, 2015 (SCI-Expanded)
- XIV. **Energy reduction in 3D NoCs through communication optimization**
Ozturk O., AKTURK I., KADAYIF İ., Tosun S.
COMPUTING, vol.97, no.6, pp.593-609, 2015 (SCI-Expanded)
- XV. **Application mapping algorithms for mesh-based network-on-chip architectures**

- TOSUN S., Ozturk O., Ozkan E., Ozen M.
 JOURNAL OF SUPERCOMPUTING, vol.71, no.3, pp.995-1017, 2015 (SCI-Expanded)
- XVI. **Energy- and reliability-aware task scheduling onto heterogeneous MPSoC architectures**
 Tosun S.
 JOURNAL OF SUPERCOMPUTING, vol.62, no.1, pp.265-289, 2012 (SCI-Expanded)
- XVII. **Application-specific topology generation algorithms for network-on-chip design**
 Tosun S., Ar Y., Ozdemir S.
 IET COMPUTERS AND DIGITAL TECHNIQUES, vol.6, no.5, pp.318-333, 2012 (SCI-Expanded)
- XVIII. **Cluster-based application mapping method for Network-on-Chip**
 Tosun S.
 ADVANCES IN ENGINEERING SOFTWARE, vol.42, no.10, pp.868-874, 2011 (SCI-Expanded)
- XIX. **New heuristic algorithms for energy aware application mapping and routing on mesh-based NoCs**
 Tosun S.
 JOURNAL OF SYSTEMS ARCHITECTURE, vol.57, no.1, pp.69-78, 2011 (SCI-Expanded)
- XX. **FIT: Fast Irregular Topology generation algorithm for application specific NoCs**
 Tosun S.
 IEICE ELECTRONICS EXPRESS, vol.7, no.15, pp.1132-1138, 2010 (SCI-Expanded)
- XXI. **Diagnosis of heart disease using artificial immune recognition system and fuzzy weighted pre-processing**
 POLAT K., GÜNEŞ S., Tosun S.
 PATTERN RECOGNITION, vol.39, no.11, pp.2186-2193, 2006 (SCI-Expanded)

Articles Published in Other Journals

- I. **Im Improving Memory proving Space Utilization in Multi coreEmbedded Systems using Task Recomputation**
 KOÇ H., TOSUN S., ÖZTÜRK Ö., KANDEMİR M. T.
 International Journal of Computer Science and Network (IJCSN), vol.1, pp.27-35, 2012 (Peer-Reviewed Journal)
- II. **Hilbert Curve Based Bucket Ordering for Global Illumination**
 YAVUZ Y., TUĞRUL B., TOSUN S.
 Journal of Computing, vol.2, pp.6-13, 2010 (Peer-Reviewed Journal)
- III. **Formal verification of pipelined synthesized designs by exploiting intermediary RTLs**
 KİM Y., Tosun S., KOÇ H., KOPURİ S., MANSOURİ N.
 International Journal of Modelling and Simulation, vol.25, no.3, pp.210-220, 2005 (Scopus)

Books & Book Chapters

- I. **Enabling Network Security in HPC Systems Using Heterogeneous CMPs**
 ÖZTÜRK Ö., TOSUN S.
 in: High Performance Computing on Complex Environments, Emmanuel Jeannot, Julius Zilinskas, Editor, John Wiley and Sons, pp.383-400, 2014
- II. **Taking Advantage of Heterogeneous Platforms in Image and Video Processing**
 MAHMOUDİ S. A., OZKAN E., MANNEBACK P., TOSUN S.
 in: High Performance Computing on Complex Environments, Emmanuel Jeannot, Julius Zilinskas, Editor, John Wiley and Sons, pp.429-450, 2014

Refereed Congress / Symposium Publications in Proceedings

- I. **Towards QoS-Aware Resource Allocation in Fog Computing: A Theoretical Model**
DİLEK S., Oracevic A., TOSUN S., ÖZDEMİR S.
2022 International Symposium on Networks, Computers and Communications, ISNCC 2022, Shenzhen, China, 19 - 21 July 2022
- II. **Q-Learning-based Routing Algorithm for 3D Network-on-Chips**
Bolucu N., TOSUN S.
24th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), ELECTRONIC NETWORK, 7 - 09 April 2021, pp.33-36
- III. **Number Analysis and Operator Detection in Telecommunication Systems**
Berk M., Aycicek O., Ay I., Gonenc S., TOSUN S.
International Symposium on Networks, Computers and Communications (ISNCC), İstanbul, Turkey, 18 - 20 June 2019
- IV. **A Distant Augmented Reality System for Cultural Heritage Sites using Drones**
ÜNAL M., BOSTANCI G. E., SERTALP E., TOSUN S.
3rd Global Summit and Expo on Multimedia and Artificial Intelligence, 20 - 21 July 2017
- V. **Energy-Aware Application-Specific Topology Generation for 3D Network-on-Chips**
BANZİNMEHR A., TOSUN S.
2017 20TH IEEE INTERNATIONAL SYMPOSIUM ON DESIGN AND DIAGNOSTICS OF ELECTRONIC CIRCUIT SYSTEMS (DDECS), Dresden, Germany, 19 - 21 April 2017, pp.84-87
- VI. **Improving Combinational Circuit Resilience against Soft Errors via Selective Resource Allocation**
YARAN T., TOSUN S.
2017 20TH IEEE INTERNATIONAL SYMPOSIUM ON DESIGN AND DIAGNOSTICS OF ELECTRONIC CIRCUIT SYSTEMS (DDECS), Dresden, Germany, 19 - 21 April 2017, pp.12-15
- VII. **FPGA implementation of a fault-tolerant application-specific NoC design**
Yesil S., TOSUN S., Ozturk O.
11th IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2016, İstanbul, Turkey, 12 - 14 April 2016
- VIII. **Moving object detection by a mounted moving camera**
Sincan O. M., Ajabshir V. B., Keles H., TOSUN S.
International Conference on Computer as a Tool, IEEE EUROCON 2015, Salamanca, Spain, 8 - 11 September 2015
- IX. **Moving Object Detection by a Mounted Moving Camera**
Sincan O. M., Ajabshir V. B., Keles H., TOSUN S.
International Conference on Computer as a Tool (EUROCON), IEEE, Salamanca, Mexico, 8 - 11 September 2015, pp.334-339
- X. **Fault-Tolerant Irregular Topology Design Method for Network-on-Chips**
Tosun S., Ajabshir V. B., Mercanoglu O., Ozturk O.
17th Euromicro Conference on Digital System Design (DSD), Verona, Italy, 27 - 29 August 2014, pp.631-634
- XI. **Fault-Tolerant Routing for Irregular-Topology-based Network-on-Chips**
Ajabshir V. B., TOSUN S.
International Symposium on Computing and Networking CANDAR, Shizuoka, Japan, 10 - 12 December 2014, pp.123-129
- XII. **Power-aware topology generation for application specific NoC design**
Tosun S., Ar Y., Ozdemir S.
2012 6th International Conference on Application of Information and Communication Technologies, AICT 2012, Tbilisi, Georgia, 17 - 19 October 2012
- XIII. **Genetic algorithm based NoC design with voltage/frequency islands**
Ozen M., Tosun S.
2011 5th International Conference on Application of Information and Communication Technologies, AICT 2011, Baku, Azerbaijan, 12 - 14 October 2011
- XIV. **TopGen: A new algorithm for automatic topology generation for network on chip architectures to reduce power consumption**

Ar Y., Tosun S., Kaplan H.

2009 International Conference on Application of Information and Communication Technologies, AICT 2009, Baku, Azerbaijan, 14 - 16 October 2009

- XV. **An ILP formulation for application mapping onto Network-on-Chips**
Tosun S., Ozturk O., Ozen M.
2009 International Conference on Application of Information and Communication Technologies, AICT 2009, Baku, Azerbaijan, 14 - 16 October 2009
- XVI. **Parallelization of render engine for global illumination of graphics scenes**
Yavuz Y., Tosun S.
2009 International Conference on Application of Information and Communication Technologies, AICT 2009, Baku, Azerbaijan, 14 - 16 October 2009
- XVII. **Foton Haritalama Algoritmasının Evrensel Aydınlatma Amaçlı ParallelestirilmesiParallelization of Photon Mapping Algorithm for Global Illumination**
YAVUZ Y., TOSUN S.
The National Symposium on Electrical-Electronics and Computer Engineering, ELECO 2008, Turkey, 26 - 30 November 2008
- XVIII. **Yonga Üstü Heterojen Çok işlemciler için Enerji Verimli s Parçacığı EslemesiTask Scheduling On Heterogeneous Chip Multiprocessors for Reducing Energy**
TOSUN S., YAVUZ Y.
The National Symposium on Electrical-Electronics and Computer Engineering, ELECO 2008, Turkey, 26 - 30 November 2008
- XIX. **Multi-level on-chip memory hierarchy design for embedded chip multiprocessors**
OZTURK O., KANDEMİR M., Irwin M. J., Tosun S.
12th International Conference on Parallel and Distributed Systems, ICPADS 2006, Minneapolis, MN, United States Of America, 12 - 15 July 2006, vol.1, pp.383-390
- XX. **An ILP Formulation for Task Scheduling on Heterogeneous Chip Multiprocessors**
TOSUN S., MANSOURİ N., KANDEMİR M., ÖZTÜRK Ö.
Computer and Information Sciences – ISCIS 2006, 1 - 03 November 2006, vol.4263, pp.267-276
- XXI. **Reducing memory requirements through task recomputation in embedded multi-CPU systems**
KOÇ H., Tosun S., OZTURK O., KANDEMİR M.
IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures 2006, Karlsruhe, Germany, 2 - 03 March 2006, vol.2006, pp.448-449
- XXII. **A Novel Essential Prime Implicant Identification Method for Exact Direct Cover Logic Minimization**
KAHRAMANLI Ş., TOSUN S.
International Conference on Computer Design & Conference on Computing in Nanotechnology, CDES 2006, 26 - 29 June 2006
- XXIII. **Using Task Recomputation During Application Mapping in Parallel Embedded Architectures**
TOSUN S., KANDEMİR M., KOÇ H.
International Conference on Computer Design & Conference on Computing in Nanotechnology, CDES 2006, 26 - 29 June 2006
- XXIV. **An ILP based approach to address code generation for digital signal processors**
ÖZTÜRK Ö., KANDEMİR M., TOSUN S.
Proceedings of the 16th ACM Great Lakes symposium on VLSI - GLSVLSI '06, Philadelphia, PA, USA, 30 April - 01 May 2006
- XXV. **Reliability-conscious process scheduling under performance constraints in FPGA-based embedded systems**
CHEN G., KANDEMİR M., Tosun S., Sezer U.
19th IEEE International Parallel and Distributed Processing Symposium, IPDPS 2005, Denver, CO, United States Of America, 4 - 08 April 2005, vol.2005
- XXVI. **On Chip Memory Management for Embedded MpSoC Architectures Based on Data Compression**
ÖZTÜRK Ö., KANDEMİR M., IRWIN M. J., TOSUN S.

- 2005 Joint 30th International Conference on Infrared and Millimeter Waves and 13th International Conference on Terahertz Electronics, Herndon, VA, USA, 19 - 23 September 2005
- XXVII. **Constraint based Code mapping for heterogeneous Chip multiprocessors**
TOSUN S., MANSOURİ N., KANDEMİR M., ÖZTÜRK Ö.
2005 Joint 30th International Conference on Infrared and Millimeter Waves and 13th International Conference on Terahertz Electronics, Herndon, VA, USA, 19 - 23 September 2005
- XXVIII. **An ILP formulation for reliability-oriented high-level synthesis**
Tosun S., OZTURK O., MANSOURİ N., ARVAS E., KANDEMİR M., XIE Y., HUNG W.
6th International Symposium on Quality Electronic Design, San-Jose, Costa Rica, 21 - 23 March 2005, pp.364-369
- XXIX. **Reliability-centric hardware/software co-design**
Tosun S., Mansouni N., ARVAS E., KANDEMİR M., XIE Y., HUNG W.
6th International Symposium on Quality Electronic Design, San-Jose, Costa Rica, 21 - 23 March 2005, pp.375-380
- XXX. **Reliability-centric high-level synthesis**
Tosun S., MANSOURİ N., ARVAS E., KANDEMİR M., XIE Y.
Design, Automation and Test in Europe Conference and Exhibition (DATE 05), Munich, Germany, 7 - 11 March 2005, pp.1258-1263
- XXXI. **Deriving Intermediary RTLs for Verification of Pipelined Synthesized Designs**
TOSUN S., KOÇ H., MANSOURİ N.
International Conference on VLSI (VLSI'03), 23 - 26 July 2003

Supported Projects

- TOSUN S., Barzinmehr A., Project Supported by Higher Education Institutions, 3D Yonga üstü Ağlar için Enerji Farkındalıklı Uygulamaya Özgü Topoloji Oluşturma, 2017 - 2017
- TOSUN S., ÖZTÜRK Ö., YEŞİL Ş., Project Supported by Higher Education Institutions, Hata Kaldırabilen Uygulamaya Özgü NoC Tasarımının FPGA Gerçekleştirimi, 2016 - 2016
- TOSUN S., Industrial Thesis Project, Algılayıcı Ağı ve Kamera Temelli Hibrid Kritik Alan İzleme Sistemi Geliştirilmesi, 2013 - 2016
- TOSUN S., TUBITAK Project, Fault Tolerant Network on Chip Architecture Design, 2013 - 2014
- TOSUN S., TUBITAK Project, Energy Efficient Application Mapping onto NoCs with Different Topologies, 2009 - 2012

Metrics

- Publication: 57
Citation (WoS): 323
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